RF and Sync Output Timing Characteristics – revC (revB).

- No programmable delay can be applied between the image clock and the RF output packet on Channels 1..4.

- A user programmable delay can be applied between the image clock and the SDIO outs on J7.

The SDIO delay feature is demonstrated below using the Isomet Studio GUI and a 121-point image.

Notes:

- Channel scoped Compensation table is applied.

- To replicate an X-Y deflector application, the Image data is programmed as follows:
  Frequency: Ch1 = Ch2, Ch3 = Ch4, and Ch1 ≠ Ch3
  Amplitude: Ch1 = Ch2, Ch3 = Ch4, and Ch1 ≠ Ch3

- External Trigger at ~3KHz

- External Clock, as noted below.

- SDIO digital sync data outputs on J7 are inverted with respect to the Image file data value.

  Bits-0…3 support < 2MHz Image data rates
  Bits-4…11 support < 1.4MHz Image data rates

To aid illustration:

- The Image amplitude data is programmed to alternate between a high and a low level.

- Image comprises 121 points; 101 active “scan” points, followed by 20 “Off” points at amplitude < 1%

Specifically, in this example:

Ch1, Ch2 Active sweep; 90-130MHz, max amplitude = 100%, low amplitude = 50%, “Off” amplitude; 0% set with a frequency of 131MHz

Ch3, Ch4 Active sweep; 85-125MHz, max amplitude = 99%, low amplitude = 0%, “Off” amplitude; 1% set with a frequency of 126MHz

Unless stated, oscilloscope channels signals are: C4 = External trigger or SDIO bit-11, as stated.
C3 = SDIO, bit-0.
C2 = External clock
C1 = RF output, J1

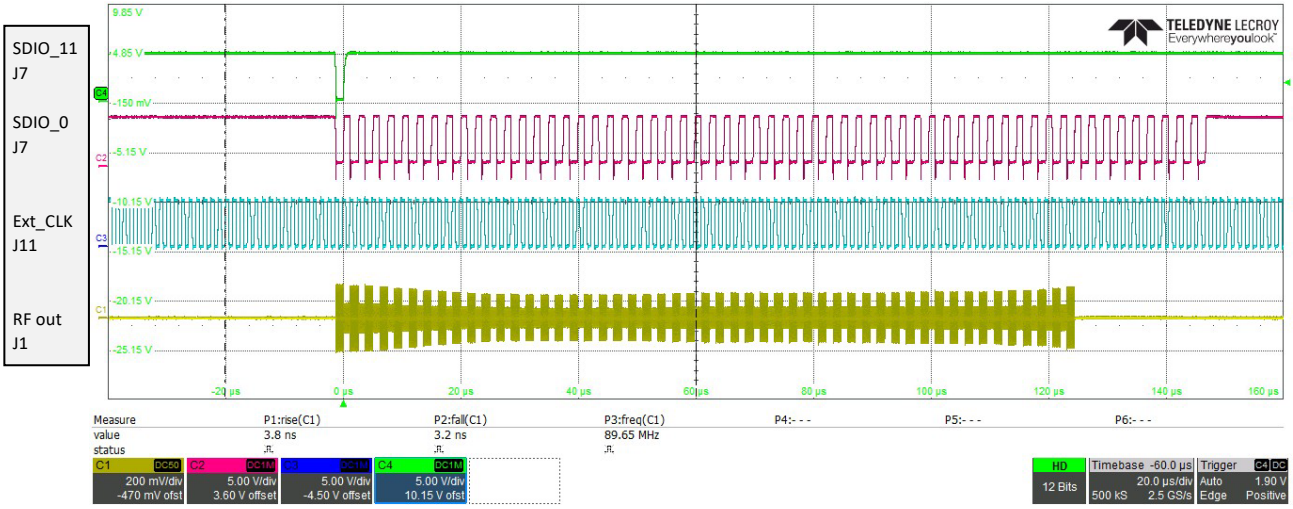
Default positive edge active is selected on external clock and trigger inputs.

IN ALL MODES:
There is a static latency (or pipe-line) delay of ~1.35usec between the external clock input edge and its corresponding image point outputs, irrespective of the clock rate (see page 3).

In the plots below the first active clock edge after a valid external trigger is indicated with ↑

For reference: a plot of the full 121-point image

Ext-clock rate ~1MHz.

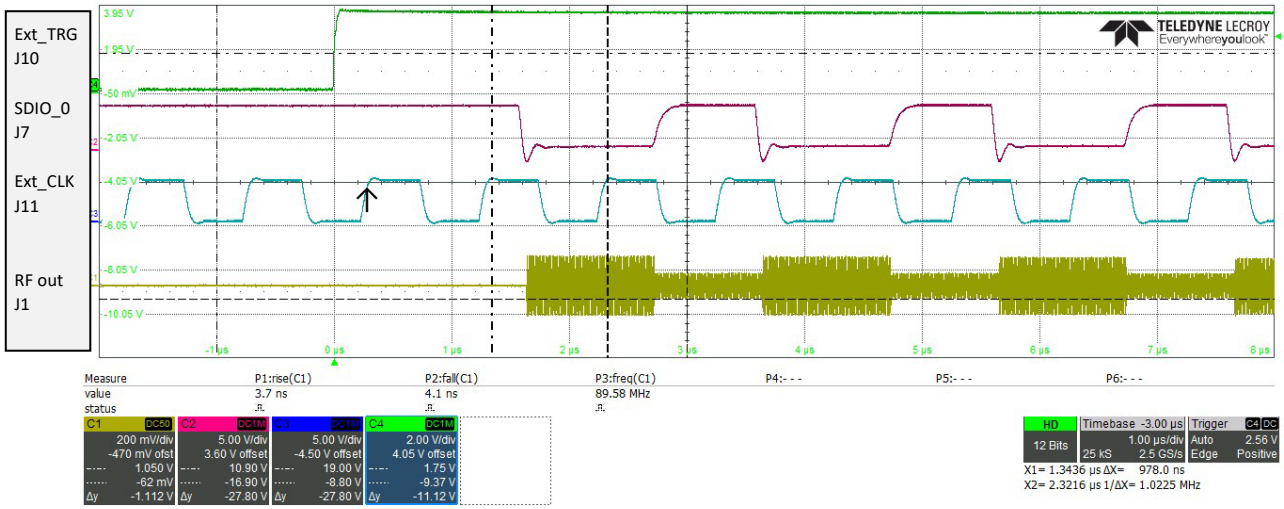


- **External Trigger - Output Jitter**

Jitter = one external clock period (plus the static ~1.35usec latency)

Ext-clock rate 1MHz

Cursors indicate min-max jitter range.

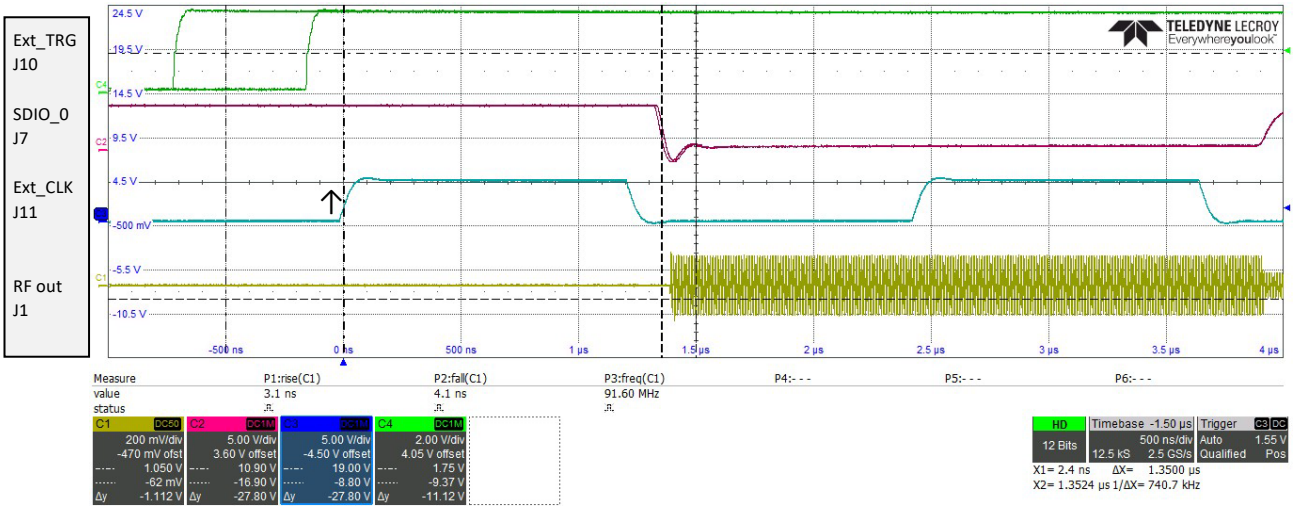


Note: In this example, the external clock period (1usec) is < latency delay (1.35us).
Hence the active clock edge for Image point-0 is the 2nd edge back from the RF output, as indicated by '↑' above.

Ext-clock rate 400KHz.

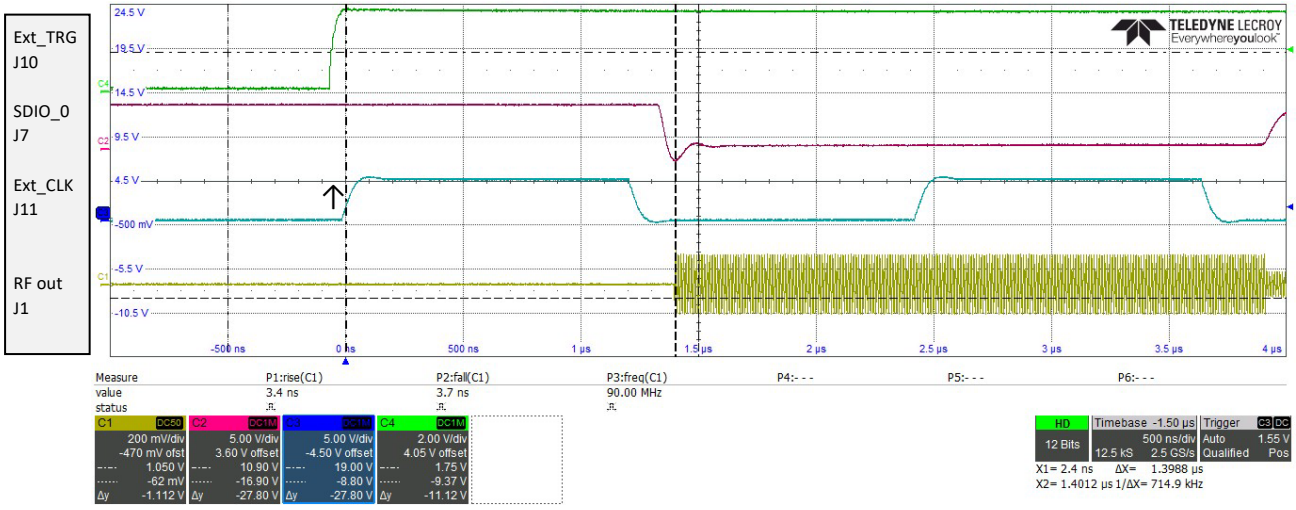
- **External clock – SDIO Output delay**

Note: the latency / pipeline delay of 1.35usec.

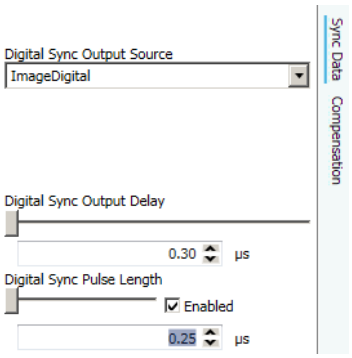


- **External clock – RF Output**

Total delay = 1.4usec. ~50nsec later than SDIO output



- **Sync Output = Pulsed mode**



The default is level mode.

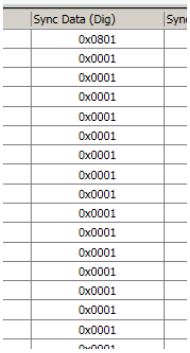
To generate a pulse output per image point

Select source = *ImageDigital*

CHECK Digital Sync Pulse Length ***Enabled*** box

Input a ***Digital Sync Pulse Length*** (usec)
MUST be less than external clock period

In this example, a low output pulse
on J7 bit-0 is required on every image point.



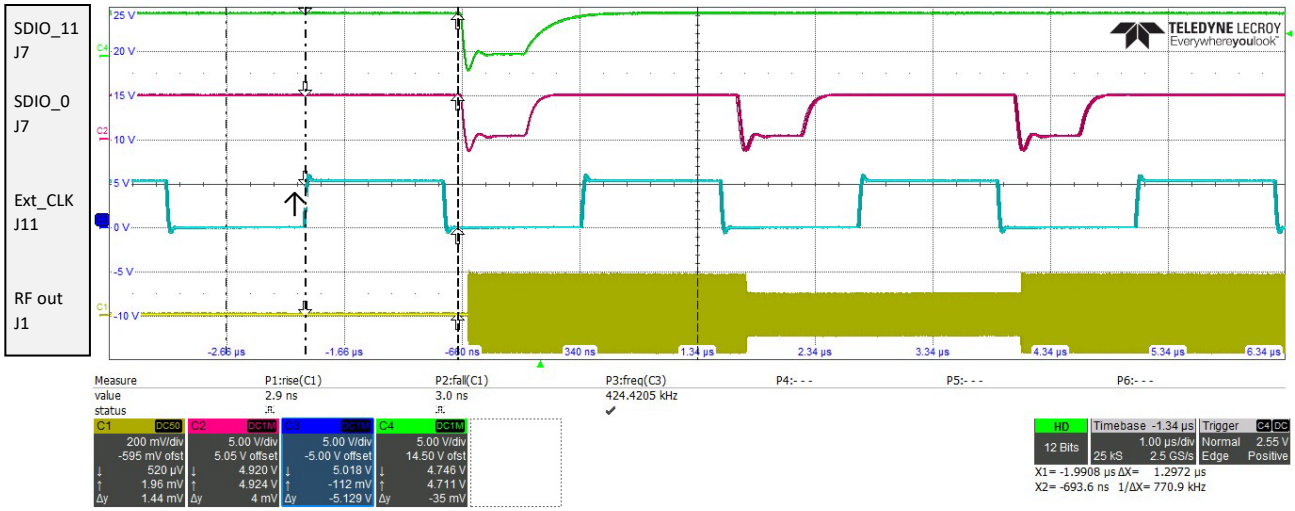
- Bit-0 is programmed 0x0001, all points.
  (Data bit high = low at J7 output)

Also

- Bit-11 programmed but on first Image point only = 0x0801

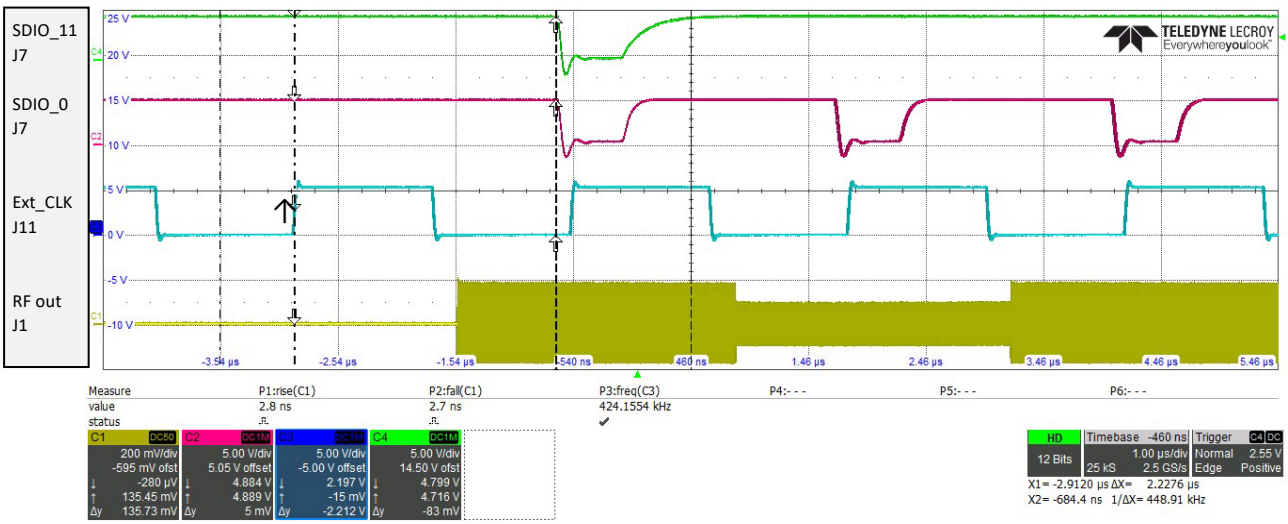
Examples:

- **Pulse enabled, 0.0usec delay, pulse length = 0.5usec**



Note: the fixed 1.35usec latency from rising clock edge ↑ to the active low SDIO output

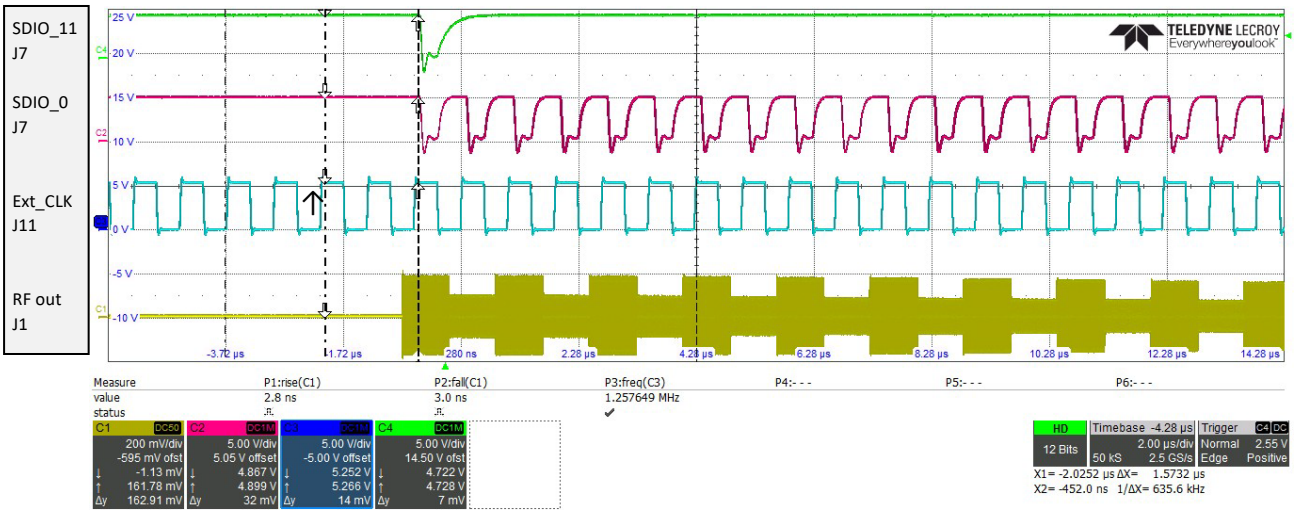
- **Pulse enabled, 0.9usec delay, pulse length = 0.5usec**



Note: total delay from rising clock edge ↑ to active low output = 1.35 latency + 0.9usec = 2.2usec

- **Pulse enabled, 0.3usec delay, pulse length = 0.25usec**

  External Clock: 1.2MHz



Note: total delay from rising clock edge ↑ to active output = 1.35 latency + 0.3sec = 1.6usec.

1.2MHz is the maximum design rate for SDIO opto-coupled outputs SDIO bits 5 – 11.
SDIO bits 0 – 4 are hardware modified to allow output > 1.5MHz.

- **Maximum 2MHz rate SDIO output rate**

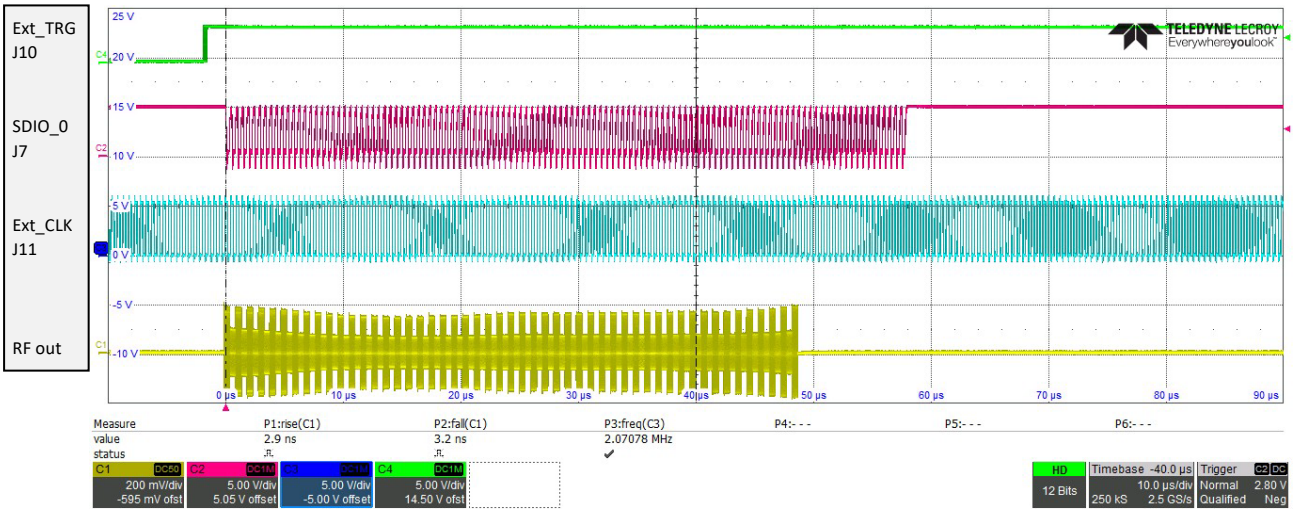
2022-2-16 We have identified an issue with SDIO output when operating at Image clock rates above 1MHz, especially when the SDIO is programmed to change frequently within an image . This does not affect the RF outputs, which are still Ok up to the maximum of 2.0MHz.

For guaranteed solid SDIO output with v3.2.90 or earlier firmware, the maximum image clock rate is 1.51MHz.
Above 1.5MHz, up to 2MHz, we cannot guarantee error free SDIO outputs.

- If the SDIO is not performing a critical function, this limitation may not be an issue.
- Depending on the application and how the SDIO is programmed, there may be few/no errors, but not with certainty.

Unfortunately, there is no in-field repair or software work-around.
If guaranteed solid SDIO output up to the maximum 2MHz is desired, the iMS4 revC needs to returned to Isomet UK for reprogramming of the synthesizer firmware to v3.2.91

- **Pulse <u>enabled</u>, 0.2usec delay, pulse length = 0.2usec**
  External Clock: 2.0MHz



To compare

- **Pulse <u>disabled</u>,**
  External Clock: 2.0MHz